WE CLAIM:

1. A method for testing a semiconductor device comprising the steps of:

providing a pin receptacle in a test board adjacent to a contact surface of the device;

interposing a pin between the pin receptacle and the contact surface of the device, the pin thereby making electrical contact between the contact surface of the device and the pin receptacle of the test pad; and

measuring an electrical signal in the device using the electrical contact between the pin receptacle and pin.

2. A method according to claim 1 wherein the step of measuring further comprises the step of measuring an electrical signal having a frequency greater than 1 GHz.

3. A method according to claim 1 wherein the step of providing a pin receptacle further comprises the step of drilling the test board.

4. A method according to claim 1 wherein the step of providing a pin receptacle further comprises the step of etching the test board.

5. A method according to claim 1 wherein the step of providing a pin receptacle

further comprises the step of depositing a metal layer on the test board.

6. A system for testing a singulated semiconductor device (DUT) comprising:

a socket for receiving a DUT, the socket having pins with ends for making electrical contact with the DUT and opposing ends for making contact with a test board;

a test board adjoining the socket, the test board having pin receptacles for receiving the opposing ends of the pins; and

measuring means operably coupled to the test board pin receptacles for measuring electrical signals in the DUT.

7. A system according to claim 6 wherein the receptacles each further comprise a basin for receiving the pin.

8. A system according to claim 6 wherein the receptacles each further comprise a generally conical basin for receiving the pin.

9. A system according to claim 6 wherein the receptacles each further comprise a generally hemispherical basin for receiving the pin.

10. A system according to claim 6 wherein the receptacles each further comprise a precision drilled basin.

11. A system according to claim 6 wherein the receptacles each further comprise an etched basin.

12. A test board for use in association with semiconductor device automatic test equipment (ATE) and a socket, the socket having pins and adapted for receiving a device under test (DUT), the test board comprising:

a contact area for operably coupling a pin to the ATE;

a pin receptacle on the contact area for receiving a pin, for thereby making staunch electrical contact between the pin and contact point.

13. A test board according to claim 12 wherein the pin receptacle further comprises a basin for receiving the pin.

14. A test board according to claim 12 wherein the pin receptacle further comprises a generally conical basin for receiving the pin.

15. A test board according to claim 12 wherein the pin receptacle further comprises a generally hemispherical basin for receiving the pin.

16. A method for probe testing a semiconductor device comprising the steps of:

providing a probe receptacle at a contact surface on the semiconductor device;

inserting a probe into the probe receptacle, thereby making electrical contact between the probe receptacle and probe; and

measuring an electrical signal in the device using the electrical contact between the probe receptacle and probe.

17. A semiconductor device comprising:

a plurality of contact surfaces; and

a probe receptacle situated on each of a plurality of the contact surfaces, each probe receptacle adapted for receiving a test probe.

18. The semiconductor device according to claim 17 wherein the probe receptacles further comprise deposited basins.

19. The semiconductor device according to claim 17 wherein the probe receptacles further comprise etched basins.